Notice of Allowability	Application No.	Applicant(s)	
	09/930,102	ANG ET AL.	
	Examiner	Art Unit	
	Habte Mered	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *14 November 2005*.

2. ☒ The allowed claim(s) is/are *1-15,17,18,20 and 22-26*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20051130* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Attachment A-Claim Listings*.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Edmund P. Pfleger on 30 November 2005.

2. The claims have been amended as shown in Attachment A.

Allowable Subject Matter

3. **Claims 1-15, 17, 18, 20 and 22-26** are allowed.

4. The following is an examiner's statement of reasons for allowance.

5. **Claims 1-9** are allowable over the prior art of record since the cited references, taken individually or in combination, fail to particularly teach or suggest a temporary storage device for receiving information in association with the line clock signal and the device comprising a first buffer receiving a first portion of the information and a second buffer receiving a second portion of the information and a pointer processor coupled to the first buffer to receive the first portion of the information, the pointer processor having a third buffer for storing the first portion of the information. It is noted that the closest prior art, Dallabetta et al (US 6, 693, 918) discloses first and second buffers with line clock decoupling means and a means to synchronously clock out data from the first and second buffers using a system clock.

6. **Claims 10-14** are allowable over the prior art of record since the cited references, taken individually or in combination, fail to particularly teach or suggest a network node comprising a receive line interface and buffers configured to decouple a line clock signal from input data and to couple a system clock signal to a first and second output data and a pointer core coupled to receive the first output data from a first buffer of the buffers synchronous to the system clock signal, the pointer core having a pointer core associated buffer configured for synchronous operation with the system clock signal on an input and output side. It is noted that the closest prior art, Dallabetta et al (US 6, 693, 918) discloses first and second buffers with line clock decoupling means and a means to synchronously clock out data from the first and second buffers using a system clock.

7. **Claim 15** is allowable over the prior art of record since the cited references, taken individually or in combination, fail to particularly teach or suggest a network comprising a first network node, a second network node, and a communication link between the nodes and a first node configured with a receive buffer and the receive buffer is located on an input data path in advance of a pointer processor buffer, where the receive buffer receives a system clock signal to clock out stored information synchronous to the clock signal. It is noted that the closest prior art, Dallabetta et al (US 6, 693, 918) discloses first and second buffers with line clock decoupling means and a means to synchronously clock out data from the first and second buffers using a system clock.

8. **Claim 17** is allowable over the prior art of record since the cited references, taken individually or in combination, fail to particularly teach or suggest a method for avoiding asynchronous pointer processing comprising providing a first and second buffer where a frame structure is clocked to a line clock to the first buffer and a frame structure is clocked to a line to a second buffer where a the first portion of the frame structure is stored in the first buffer and the second portion of the frame structure is stored in the second buffer and a step of providing the first portion and the second portion of the frame structure from the first buffer and the second buffer to a pointer processor buffer; and clocking out with a pulse signal synchronized with the system clock signal the first portion and the second portion of the frame structure from the pointer processor. It is noted that the closest prior art, Dallabetta et al (US 6, 693, 918) discloses first and second buffers with line clock decoupling means and a means to synchronously clock out data from the first and second buffers using a system clock.

9. **Claim 18** is allowable over the prior art of record since the cited references, taken individually or in combination, fail to particularly teach or suggest a network comprising a first network node, a second network node, and a communication link between the nodes and a first node configured with a receive buffer and a transmit buffer and where the transmit buffer is located on an input data path in advance of a pointer processor buffer and the transmit buffer comprises of a frame timing generator and a temporary storage device where the data written to the temporary storage device is synchronous to the system clock signal and the data outputted from the temporary storage device is synchronous to the line clock signal. It is noted that the closest prior

art, Dallabetta et al (US 6, 693, 918) discloses first and second buffers with line clock decoupling means and a means to synchronously clock out data from the first and second buffers using a system clock.

10. **Claims 20 and 22-26** are allowable over the prior art of record since the cited references, taken individually or in combination, fail to particularly disclose fail to particularly teach or suggest a temporary storage device for receiving overhead information in association with the line clock signal and the device comprising a first buffer for receiving and storing a first portion of the overhead information and a second buffer for receiving and storing a second portion of the overhead information and a pointer processor coupled to receive the first stored overhead information, the pointer processor have a third buffer for storing the first stored overhead information. It is noted that the closest prior art, Dallabetta et al (US 6, 693, 918) discloses first and second buffers with line clock decoupling means and a means to synchronously clock out data from the first and second buffers using a system clock.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

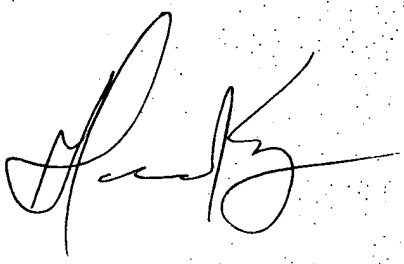
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HM
11-30-2005



HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Attachment A

Amendments to the Claims:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A temporary storage device, comprising:

a first buffer, the first buffer configured to receive information, the information provided in association with a line clock signal, the first buffer configured to receive a first write enable signal for storing a first portion of the information;

a second buffer, the second buffer configured to receive the information, the information provided in association with the line clock signal, the second buffer configured to receive a second write enable signal for storing a second portion of the information different from the first portion of the information;

a system clock signal provided to the first buffer and the second buffer for synchronously clocking out the first portion and the second portion of the information; and

a pointer processor coupled to the first buffer to receive the first portion of the information, the pointer processor ~~have~~ having a third buffer for storing the first portion of the information.

2. (Previously Presented) The temporary storage device of claim 1 further comprising coupled between the first buffer and the pointer processor, a first reader coupled to receive the first portion of the information from the first buffer and configured to provide a first read enable signal to the first buffer and to provide the first information to the pointer processor.

3. (Original) The temporary storage device of claim 2 further comprising:

combinatorial logic configured to provide the first write enable signal, the combinatorial logic configured to provide the first write enable signal in part when selected overhead signals are active;

an overhead extractor-processor configured to receive the second portion of the information; and

a second reader coupled between the overhead extractor-processor and the second buffer, the second reader coupled to receive the second portion of the information from the second buffer and configured to provide a second read enable signal to the second buffer and to provide the second portion of the information to the overhead extractor-processor.

4. (Original) The temporary storage device of claim 1 wherein the first portion of the information synchronously outputted from the first buffer consists of H1-pointer, H2-pointer and H3-pointer information and a synchronous payload envelope.

5. (Original) The temporary storage device of claim 1 wherein the second portion of the information synchronously outputted from the second buffer consists of section overhead or line overhead or a combination thereof or consists of regenerator section or multiplex section overhead or a combination thereof.

6. (Original) The temporary storage device of claim 1 wherein the second write enable signal is a transport overhead signal or a section overhead signal.

7. (Original) The temporary storage device of claim 6 wherein the second write enable signal is active for providing available columns.

8. (Original) The temporary storage device of claim 1 wherein the first portion of the information or the second portion of the information is tagged.

9. (Previously Presented) The temporary storage device of claim 1 wherein the first portion of the information or the second portion of the information is tagged with an H1-pointer byte.

10. (Previously Presented) A network node comprising:

a receive line interface configured to receive at least one transmission;

buffers configured to decouple a line clock signal from input data and to couple a system clock signal to first and second output data; and

a pointer core coupled to receive the first output data from a first buffer of the buffers synchronous to the system clock signal, the pointer core having a pointer core associated buffer configured for synchronous operation with the system clock signal on an input and an output side;

wherein the buffers include:

a first buffer configured to receive a first portion of the input data; and

a second buffer configured to receive a second portion of the input data that is different from the first portion.

11. (Original) The network node of claim 10 further comprising:

an overhead extractor-processor coupled to receive the second output data from a second buffer of the buffers synchronous to the system clock signal.

12. (Original) The network node of claim 11 further comprising:

a first multiplexer coupled to receive the first output data from the first buffer and to provide the first output data to the pointer core; and

a second multiplexer coupled to receive the second output data from the second buffer and to provide the second output data to the overhead extractor processor.

13. (Original) The network node of claim 12 wherein the multiplexers are round-robin readers clocked by the system clock signal.

14. (Previously Presented) A network node comprising:

a frame timing generator, the frame timing generator configured for synchronous operation off of a system clock signal;

a temporary storage device configured to receive data output from the frame timing generator, the temporary storage device configured to decouple the system clock

signal from the data and to couple a line clock signal to the data, the data written to the temporary storage device synchronous to the system clock signal, the data outputted from the temporary storage device synchronous to the line clock signal; and

a pointer core having a buffer, the buffer configured to receive the data output from the temporary storage device, the buffer configured to operate on both an input side and an output side synchronous with the line clock signal;

wherein the temporary storage device includes:

a first buffer configured to receive a first portion of the data output from the frame timing generator; and

a second buffer configured to receive a second portion of the data output from the frame timing generator that is different from the first portion.

15. (Currently Amended): A network comprising:

a first network node;

a second network node;

a communication link for putting the first network node in communication with the second network node;

the first network node configured with a receive buffer, the receive buffer is located on an input data path in advance of a pointer processor buffer, the receive buffer comprising:

a first buffer, the first buffer configured to receive at least a first portion of the overhead information, the at least a first portion of the overhead information provided in association with a line clock signal, the first buffer configured to store a first portion of the at least a first portion of the overhead information; and

a second buffer, the second buffer configured to receive at least a second portion of the overhead information, the at least a second portion of the overhead information provided in association with a line clock signal, the second buffer configured to store a second portion of the at least a second portion of the overhead information; and

the first buffer and the second buffer coupled to receive a system clock signal and configured to respectively clock out the first and second stored information synchronous to the system clock signal,

wherein the second portion of the overhead information is different from the first portion of the overhead information.

16. (Cancelled)

17. (Original) A method for avoiding one or more asynchronicities in pointer processing, comprising:

providing a first buffer and a second buffer;

providing a frame structure clocked to a line clock to the first buffer;

providing the frame structure clocked to the line clock to the second buffer;

storing a first portion of the frame structure in the first buffer;

storing a second portion of the frame structure in the second buffer, the second portion different from the first portion;

clocking out the first portion of the frame structure from the first buffer synchronous to a system clock signal;

clocking out the second portion of the frame structure from the second buffer synchronous to the system clock signal;

providing the first portion and the second portion of the frame structure from the first buffer and the second buffer to a pointer processor buffer; and

clocking out with a pulse signal synchronized with the system clock signal the first portion and the second portion of the frame structure from the pointer processor buffer.

18. (Currently Amended) A network comprising:

a first network node;

a second network node;

a communication link for putting the first network node in communication with the second network node;

the first network node configured with a receive buffer and a transmit buffer, the transmit buffer is located on an input data path in advance of a pointer processor buffer, the transmit buffer comprising:

a frame timing generator; and

a temporary storage device configured to receive data output from the frame timing generator, the temporary storage device configured to decouple a system clock signal from the data and to couple a line clock signal to the data, the data written to the temporary storage device synchronous to the system clock signal and outputted from the temporary storage device synchronous to the line clock signal;

wherein the temporary storage device includes:

a first buffer configured to receive a first portion of the data output from the frame timing generator; and

a second buffer configured to receive a second portion of the data output from the frame timing generator that is different from the first portion.

19. (Cancelled)

20. (Currently Amended): A temporary storage device configured to receive overhead information and data, comprising:

a first buffer, the first buffer coupled to receive at least a first portion of the overhead information, the at least a first portion of the overhead information provided in association with a line clock signal, the first buffer configured to store the at least a first portion of the overhead information to provide first stored overhead information;

a second buffer, the second buffer coupled to receive at least a second portion of the overhead information, the at least a second portion of the overhead information provided in association with the line clock signal, the second buffer configured to store the at least a second portion of the overhead information to provide second stored overhead information; ~~and~~

the first buffer and the second buffer coupled to receive a system clock signal and configured to respectively clock out the first and second stored information synchronous to the system clock signal,

wherein the second portion of the overhead information is different from the first portion of the overhead information.; and

a pointer processor coupled to receive the first stored overhead information, the pointer processor having a third buffer for storing the first stored overhead information.

21. (Cancelled)

22. (Currently Amended) The temporary storage device of claim ~~21~~ 20 further comprising a first reader coupled to receive the first stored overhead information from the first buffer and configured to provide a first read enable signal to the first buffer and to provide the first stored overhead information to the pointer processor.

23. (Original) The temporary storage device of claim 22 further comprising first combinatorial logic configured to provide a first write enable signal to select the at least a first portion of the overhead information written to the first buffer.

24. (Original) The temporary storage device of claim 23 further comprising an overhead extractor-processor coupled to receive the second stored overhead information.

25. (Original) The temporary storage device of claim 24 further comprising a second reader coupled to receive the second stored overhead information from the second buffer and configured to provide a second read enable signal to the second buffer and to provide the second stored overhead information to the overhead extractor-processor.

26. (Original) The temporary storage device of claim 25 further comprising second combinatorial logic configured to provide a second write enable signal to select the at least a second portion of the overhead information written to the second buffer.